

HEXFET® Power MOSFET

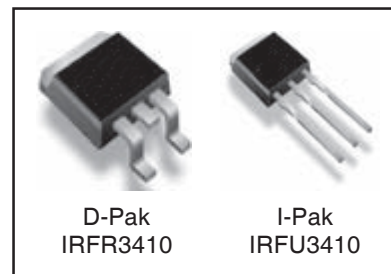
Applications

- High frequency DC-DC converters

V_{DSS}	$R_{DS(on)}$ max	I_D
100V	39mΩ	31A [Ⓢ]

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	31 [Ⓢ]	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	22	
I_{DM}	Pulsed Drain Current [Ⓢ]	125	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	110	W
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	3.0	
	Linear Derating Factor	0.71	W [Ⓢ] C
dv/dt	Peak Diode Recovery dv/dt [Ⓢ]	15	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1mA ④
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	34	39	mΩ	V _{GS} = 10V, I _D = 18A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

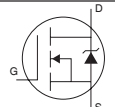
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	33	—	—	S	V _{DS} = 25V, I _D = 18A
Q _g	Total Gate Charge	—	37	56	nC	I _D = 18A V _{DS} = 50V V _{GS} = 10V, ④
Q _{gs}	Gate-to-Source Charge	—	10	—		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	11	—		
t _{d(on)}	Turn-On Delay Time	—	12	—	ns	V _{DD} = 50V I _D = 18A R _G = 9.1Ω V _{GS} = 10V ④
t _r	Rise Time	—	27	—		
t _{d(off)}	Turn-Off Delay Time	—	40	—		
t _f	Fall Time	—	13	—		
C _{iss}	Input Capacitance	—	1690	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz V _{GS} = 0V, V _{DS} = 80V, f = 1.0MHz V _{GS} = 0V, V _{DS} = 0V to 80V ⑤
C _{oss}	Output Capacitance	—	220	—		
C _{rss}	Reverse Transfer Capacitance	—	26	—		
C _{oss}	Output Capacitance	—	1640	—		
C _{oss}	Output Capacitance	—	130	—		
C _{oss eff.}	Effective Output Capacitance	—	250	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	140	mJ
I _{AR}	Avalanche Current①	—	18	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	31⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	125		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 18A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	84	—	ns	T _J = 25°C, I _F = 18A
Q _{rr}	Reverse Recovery Charge	—	260	—	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

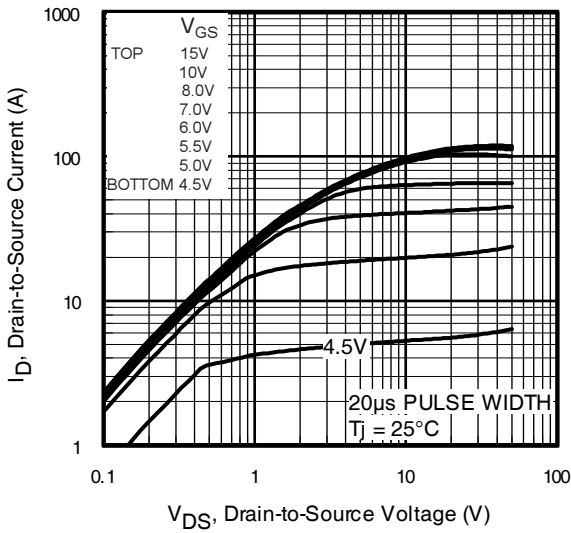


Fig 1. Typical Output Characteristics

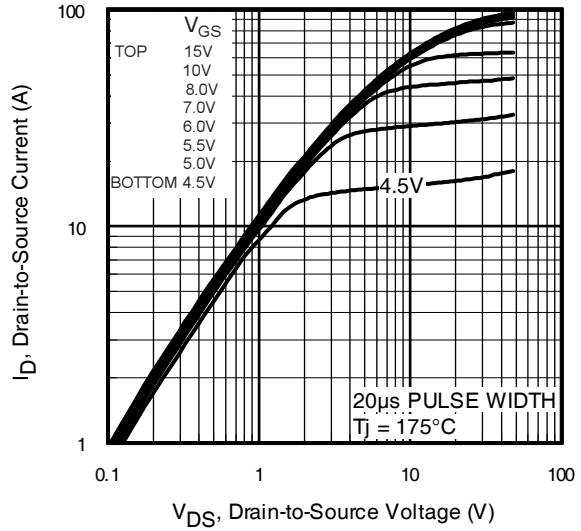


Fig 2. Typical Output Characteristics

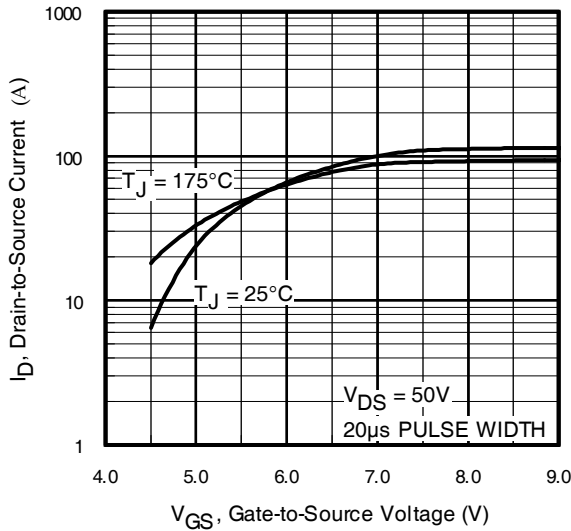


Fig 3. Typical Transfer Characteristics

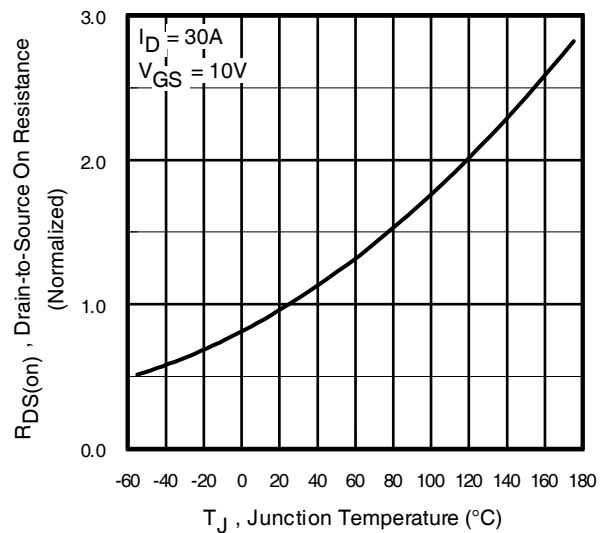


Fig 4. Normalized On-Resistance Vs. Temperature

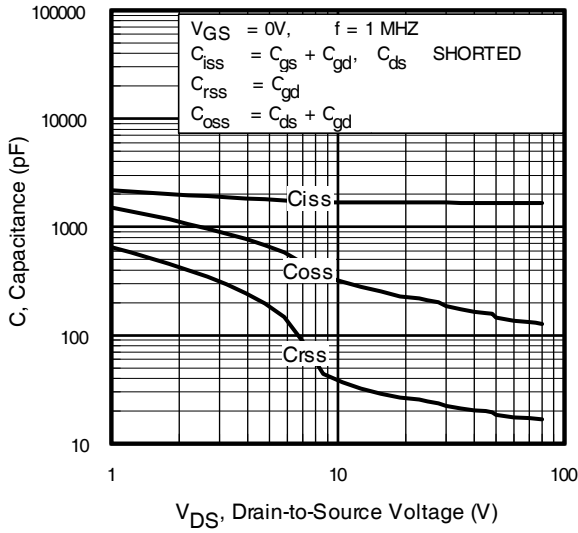


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

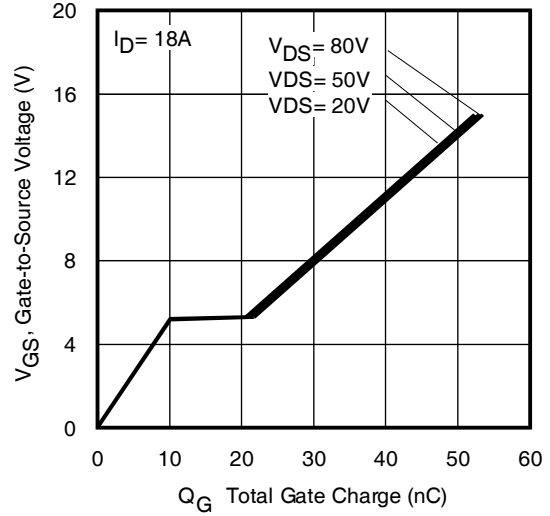


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

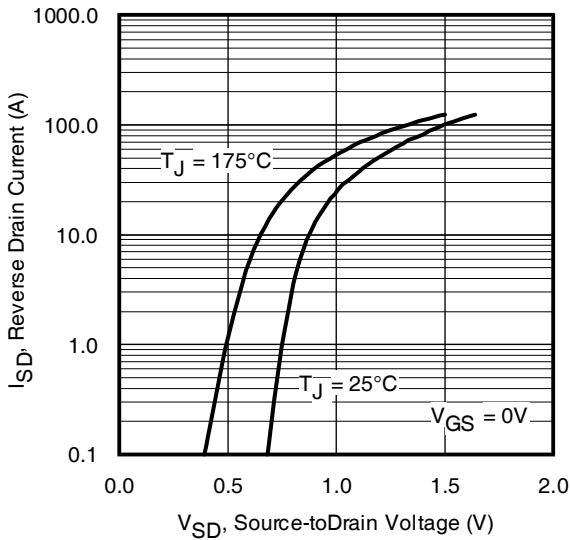


Fig 7. Typical Source-Drain Diode Forward Voltage

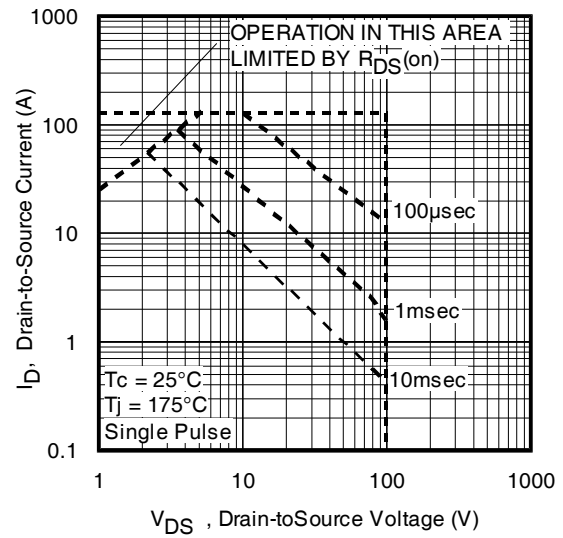


Fig 8. Maximum Safe Operating Area

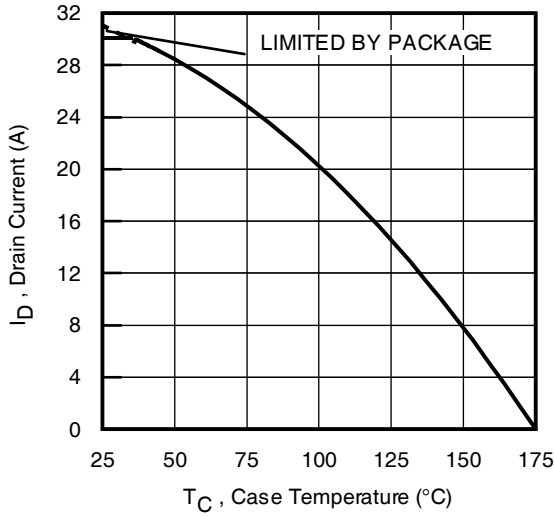


Fig 9. Maximum Drain Current Vs. Case Temperature

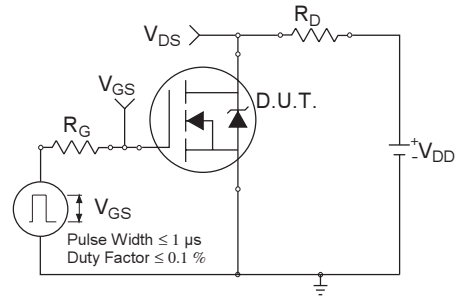


Fig 10a. Switching Time Test Circuit

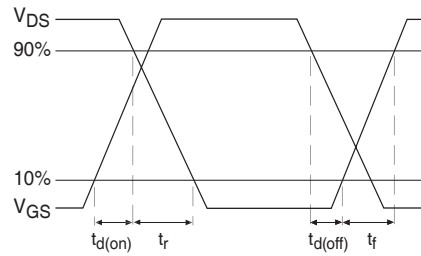


Fig 10b. Switching Time Waveforms

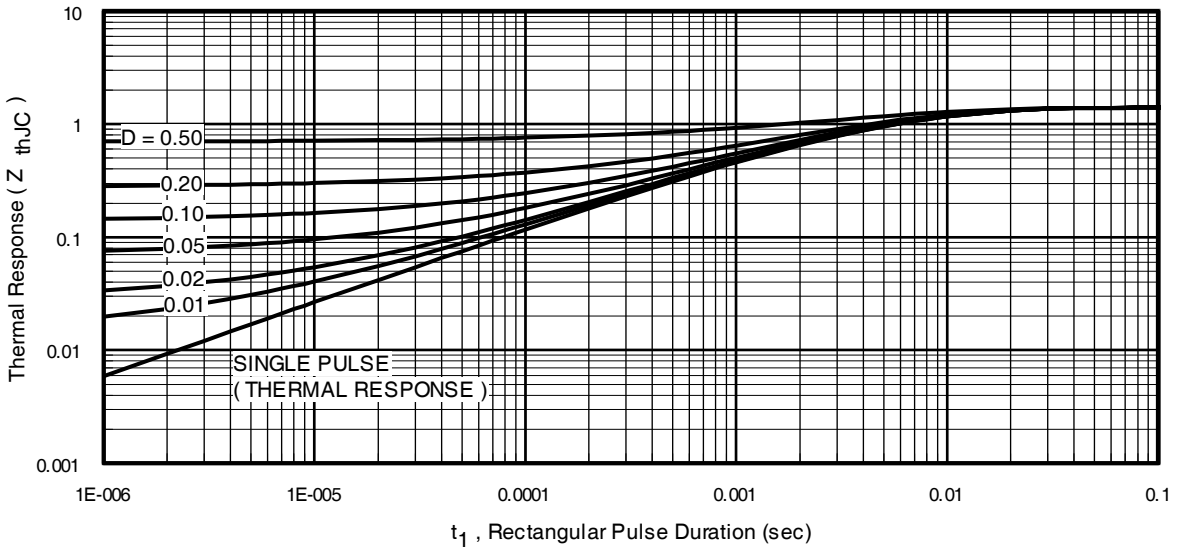


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

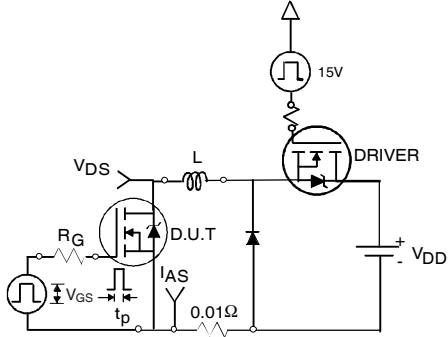


Fig 12a. Unclamped Inductive Test Circuit

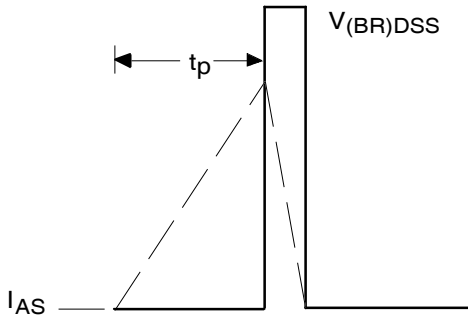


Fig 12b. Unclamped Inductive Waveforms

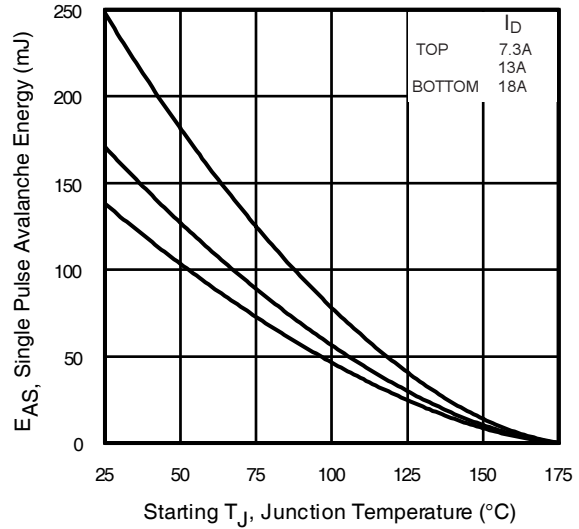


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

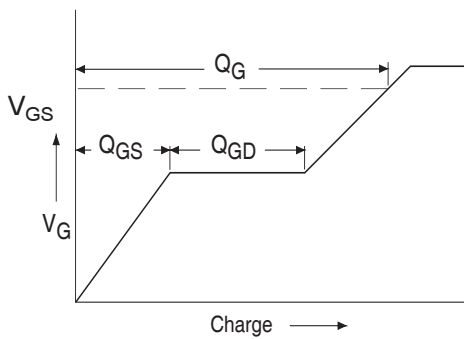


Fig 13a. Basic Gate Charge Waveform

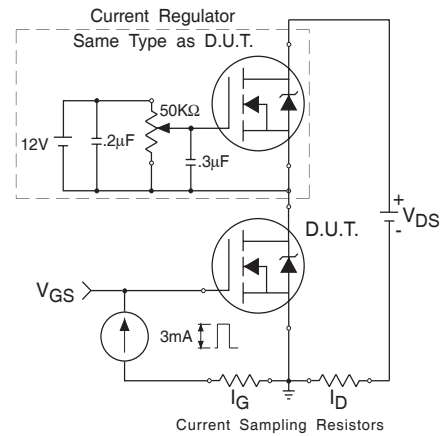
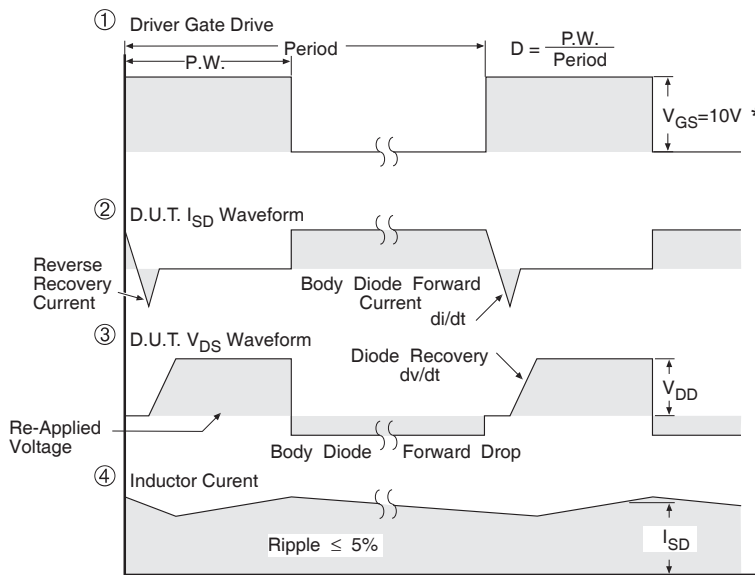
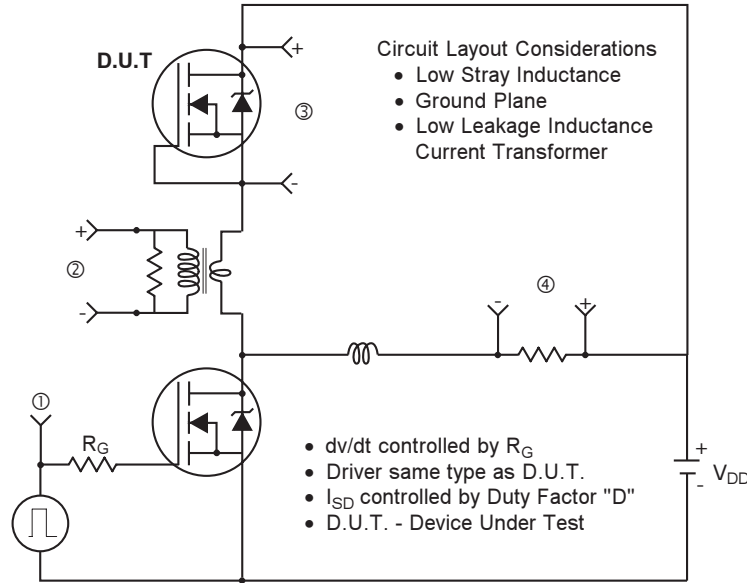


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

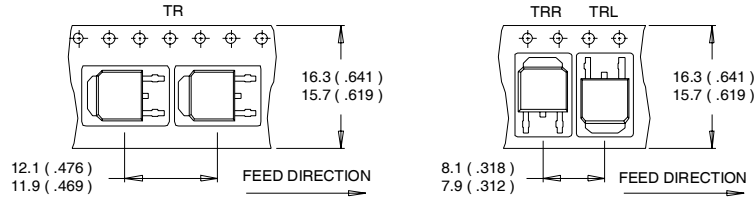


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

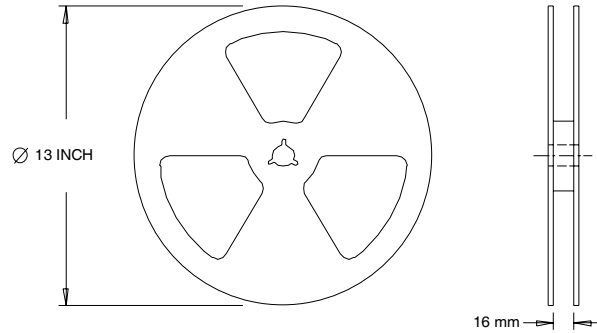
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.85\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 18\text{A}$.
- ③ $I_{SD} \leq 18\text{A}$, $di/dt \leq 360\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.